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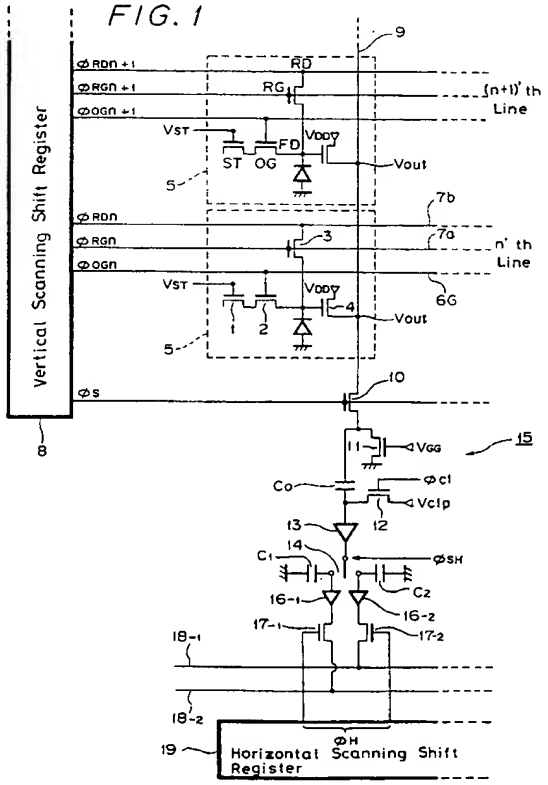
(54) Solid state imager.

(57) The solid state imager of an amplifying type having an amplifying element (4) for each photo receptor portion comprises a noise cancelling unit (15) for the amplified output of each photo receptor portion at every vertical line. The imager is rear-illuminated so that the numerical aperture and the sensitivity are improved due to a reduction of noise. Photo receptor portions (22) are provided for each of a plurality of pixels arranged in a matrix configuration in horizontal and vertical directions and each has said amplifying element (4) arranged on a major surface side of a substrate (20) for amplifying the signal charge accumulated depending on the quantity of light incident thereon. First and second signal holding units (C_1, C_2) are provided for holding during a horizontal blanking period amplified outputs of said photo receptor portions of two pixels (5) adjacent to each other in the vertical direction after passing through the noise cancelling unit (15). A signal reading unit (14-15) allows independent reading of the outputs of said first and second signal holding units (C_1, C_2).

FIG. 1



EP 0 481 373 A2

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to a solid state imager and more particularly to a solid state imager of an amplifying type having an amplifying element at every photo receptor portion.

Description of the Prior Art

In a typical conventional solid state imager using a charge coupled device (CCD), a signal charge whose amount depends on incident light quantities stored in a photoelectric converting portion of each pixel is directly transferred to an output portion by means of the CCD, so that there has been such a drawback that the signal-to-noise (S/N) ratio of the signal change is likely to be degraded since noise components are contaminated into the signal charge during the transferring thereof by the CCD.

In order to obviate this drawback of the conventional solid state imager, there has been proposed a solid state imager of an amplifying type wherein there are provided a photo receptor portion having a photoelectric converting portion for storing a signal charge whose amount depends on incident light quantities, a unit for amplifying the signal charge accumulated in the photoelectric converting portion, and a unit for resetting an input of the amplifying unit is provided for each of a plurality of pixels arranged in a matrix or two-dimensional configuration, as disclosed in, for example, Japanese Patent Laid-Open Publication No. 1-154678.

However, in this conventional amplifying type solid state imager, the fixed pattern noise due to defects of elements can be reduced by improving the manufacturing process of the imager, but the reset noise due to the characteristics etc. of the elements is hardly reduced since it is originated from the principle of the elements. Further, the conventional amplifying type solid state imager is of the front-illumimated structure, and so the numerical aperture is disadvantageously small.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide an improved solid state imager in which the aforementioned shortcomings and disadvantages of the prior art can be eliminated.

More specifically, it is an object of the present invention to provide an improved solid state imager which is capable of reducing noises and improving the numerical aperture to provide a high sensitivity.

According to an aspect of the present invention, a solid state imager is comprised of a plurality of pixels arranged in the horizontal and vertical directions in a matrix or two-dimensional configuration and each having an amplifying element, the output of which is connected to the corresponding vertical signal line; a plurality of noise cancel circuits, each being connected to the corresponding vertical signal line; a first hold unit for receiving the output signal of the n'th horizontal line during a horizontal blanking period through the noise cancel circuit; a second holding unit for receiving the output signal of the (n + 1)'th horizontal line during a horizontal blanking period through the noise cancel circuit; and a switching unit for selectively supplying the output signal of the noise cancel circuit to the first hold unit or to the second hold unit.

According to another aspect of the present invention, a solid state imager is comprised of photo receptor portions each provided for the corresponding one of a plurality of pixels arranged in a matrix configuration to the horizontal and vertical directions and each having an amplifying element provided on a major surface side of a substrate for amplifying a signal charge accumulated depending on incident light quantities incident thereon, incident light being radiated on a rear surface side of the substrate; a plurality of noise cancelling units each provided for the corresponding vertical line for cancelling noise included in the outputs of the corresponding amplifying elements; first and second signal holding units for holding during a horizontal blanking period amplified outputs of the photo receptor portions of two pixels adjacent to each other to the vertical direction passed through the noise cancelling unit; and a signal reading unit for independently reading outputs of the first and second signal holding units.

According to the solid state imager of the present invention, noises included in the amplified outputs of the respective photo receptor portions are eliminated by the noise cancel units each provided for the corresponding vertical line, and the amplified outputs of the respective photo receptor portions of the two pixels adjacent to each other to the vertical direction are held during a horizontal scanning period, and then the held amplified outputs are independently read out, whereby a non-interlace television signal can be obtained.

Further, according to the present invention, a noise cancelling unit is provided for the amplified outputs of the respective photo receptor portions of each vertical line so as to decrease noises such as the reset noise and the smear, and further the solid state imager is configured to be the rear-illuminated structure, so that the sensitivity of the solid state imager can be improved due to the reduction of the noises and the numerical aperture thereof can be also improved.

The above and other objects, features and advantages of the present invention will become apparent from the following detailed description of an illustrative embodiment thereof to be read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating a main part of a solid state imager according to an embodiment of the present invention;

FIG. 2 is a sectional view illustrating the structure of one unit cell;

FIG. 3 is a diagram illustrating the potential distribution of the one unit cell of FIG. 2;

FIG. 4 is a rear view illustrating a part of the solid state imager according to the embodiment of the present invention; and

FIGS. 5A to 5E are a timing chart for explaining the operation of the circuit of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will now be described with reference to the accompanying drawings in which like reference numerals denote like or corresponding elements throughout the drawings.

FIG. 1 is a circuit diagram illustrating a main part of a solid state imager according to an embodiment of the present invention, wherein, among a plurality of pixels arranged in a matrix configuration to horizontal and vertical directions, the circuit configuration of one pixel of each of only adjacent two lines, that is, n'th and (n + 1)'th lines is shown for the simplification of the explanation since other pixels have the same circuit configurations.

Referring to FIG. 1, when light is incident on each pixel, a signal charge whose amount depends on an incident light quantity is stored in a storage (ST) 1. The storage 1 and an output gate (OG) switch 2 connected thereto constitutes a one-bit charge coupled device (CCD). A metal oxide semiconductor field effect transistor (MOSFET) 3 for a reset operation and a source follower MOSFET 4 for an amplifying operation are formed on the same chip as the CCD, and a gate of the MOSFET 4 for the amplifying operation is connected to a floating diffusion (FD) to constitute a floating diffusion amplifier (FDA) 5.

In the floating diffusion amplifier 5, a gate electrode of the output gate switch 2 is connected to an output gate (OG) signal line 6, a gate electrode of the MOSFET 3 for the reset operation is connected to a reset gate (RG) signal line 7a, and a drain electrode thereof is connected to a a reset drain (RD) signal line 7b. A horizontal line is selected by applying from a vertical scanning shift register 8 an output gate pulse ϕ_{OG}, a reset gate pulse ϕ_{RG}, and a reset drain pulse ϕ_{RD} to the gate electrode of the output gate switch 2, the gate electrode of the MOSFET 3 for the reset operation, and the drain electrode thereof, respectively. A drain electrode of the MOSFET 4 for the amplifying operation is supplied with a power supply voltage V_{DD} and a source electrode thereof serving as an output terminal Vout is connected to a vertical signal line 9. In this configuration, when one horizontal line is selected, the signal charge of the pixel of the selected horizontal line is amplified by the MOSFET 4 for the amplifying operation to be applied to the vertical signal line 9.

A load transistor 11 is connected to the vertical signal line 9 through a transfer gate switch 10, so that the amplified signal charge of each pixel applied to the vertical signal line 9 is stored in a noise cancelling capacitor C_0 through the transfer gate switch. An output terminal of the capacitor C_0 is connected to a clamping switch 12, which is turned on in response to a clamping pulse ϕcl applied to a gate electrode thereof to thereby clamp a voltage of the output terminal of the capacitor C_0 at a clamping level Vclp. The noise cancelling capacitor C_0 and the clamping switch 12 constitute a correlated double sampling (CDS) circuit 15 for decreasing reset noise etc. included in the source output signal of the MOSFET 4.

The output signal of the noise cancelling capacitor C_0 is applied through a buffer amplifier 13 to a change-over switch 14, which in turn selectively applies the output signal to first and second signal holding units, e.g., sample-and-hold capacitors C1 and C2 to thereby sample and hold the output signal. The change-over switch 14 is controlled by a sample-and-hold pulse ϕ_{SH} generated in a horizontal blanking period such that it is alternately connected to the capacitors C1 and C2 at every one line. Thus, an output signal of a pixel on an even number line and that on an odd number line are held in these sample-and-hold capacitors, for example, capacitors C1 and C2, respectively.

The signals held in the capacitors C1 and C2 are applied through buffer amplifiers 16_{-1} and 16_{-2} to horizontal gate switches 17_{-1} and 17_{-2}, which in turn apply the signals to horizontal signal lines 18_{-1} and 18_{-2} by the switching operations thereof responding to horizontal shift pulses ϕ_H applied thereto from a horizontal scanning shift register 19, respectively.

FIG. 2 shows a cross-sectional view of the thus constituted solid state imager of the present invention, that is, a cross-sectional view of the storage (ST), output gate (OG), reset gate (RG), reset drain (RD), and drain electrode (V_{DD}), gate electrode and source electrode (Vout) of the FET 4 in one unit

cell (one-bit CCD). The FET 4 may be a junction FET instead of the MOSFET shown in FIG. 2. As clear from FIG. 2, the solid state imager according to the present invention is constituted in a manner as described below. Firstly, electrode element groups constituting the floating diffusion amplifier (FDA) are arranged on a major surface of a thin silicon substrate 20, and then an SiO_2 film 21 is deposited thereon by the chemical vapor deposition (CVD) process, etc. An SiO_2 film 22 is provided on a rear surface of the silicon substrate 20, then horizontal aluminum lines 23 and vertical aluminum lines 24 are interconnected in a matrix pattern configuration on the SiO_2 film 22 as shown in FIG. 4 to thereby connect the reset drain (RD) and the output terminal (Vout) of the amplifying MOSFET 4 to the lines 23 and 24, respectively. Thus, the solid state imager is constituted such that incident light is radiated on the rear surface side of the silicon substrate 20, that is, a rear-illuminated structure.

Thus, since the solid state imager is constructed to be the rear-illumination type, only the horizontal and vertical aluminum lines 23 and 24 are interconnected on the rear surface side of the silicon substrate 20, thereby improving a numerical aperture (NA) remarkably to provide a high sensitivity.

An operation of the one unit cell (one pixel) selected by the vertical scanning shift register 8 and the horizontal scanning shift register 19 in the solid state imager according to the present invention will be explained in accordance with a time chart in FIG. 5 with reference to the sectional diagram of the cell in FIG. 2 and a potential distribution diagram in FIG. 3.

Firstly, in a horizontal blanking period, as shown in FIG. 3, a reset voltage V_{RD} of a high level (e.g., 5 V) of the reset drain pulse ϕ_{RD} is applied at a time point t1 to the reset drain (RD) of only the n'th horizontal line to be selected in the vertical direction, while a low level voltage (e.g., 1.5 V) is applied to the reset drains of the remaining horizontal lines, whereby one horizontal line (the n'th line) is selected (refer to FIGS. 5A to 5E). At this time, the reset gate pulse ϕ_{RG} of a high level is applied to the floating diffusion FD of a pixel of the selected horizontal line to reset it, then the voltage of the floating diffusion FD becomes a high level to make the the gate electrode of the amplifying MOSFET 4 also a high level. On the other hand, the voltage of the floating diffusion FD of each pixel of the non-selected horizontal lines is kept at a low level, so that the voltage of the gate electrode of the amplifying MOSFET 4 is smaller than the voltage of the floating diffusion FD by a threshold level Vth (e.g., 0.5 V) as shown by a dotted line in FIG. 3 to place the MOSFET 4 in a cut-off state.

Then, the voltage of the reset-gate pulse ϕ_{RG} is shifted to a low level at a time point t2 to place each of the MOSFETs 3 for the reset operation in a cut-off state. In this state, the clamping switch 12 is made in the ON state by the clamping pulse ϕcl of a high level applied thereto to thereby clamp the output terminal of the capacitor C_0 at the clamping level Vclp. When the clamping pulse ϕcl is shifted to a low level at a time point t3 or disappears, the clamping switch 12 is turned off.

The capacitor C_0 and the clamping switch 12 of the CDS circuit 15 can cancel a fixed pattern noise (FPN) due to defects of elements, fluctuation of the threshold level Vth due to variations of the offset input to the source follower MOSFET 4, low frequency (l/f) noise of the source follower, reset noise generated in resetting the FDA, and smear due to incident light on the signal lines and the CCDs, whereby a frame memory which has been used in a signal processing system in order to eliminate the fixed pattern noise of the prior art can be removed.

Thereafter, the output gate (OG) 2 is turned on in response to the output gate pulse ϕ_{OG} of a high level at a time point t4 to thereby start transferring the signal charge stored in the storage (ST)1 to the floating diffusion (FD) so that all signal charge stored in the storage is transferred to the FD until the output gate pulse ϕ_{OG} becomes low level or disappears at a time point t5. The change-over switch 14 is then changed over to the sample-and-hold capacitor C1 side in response to the sample-and-hold pulse ϕ_{SH} of a high level at a time point t6 to thereby apply the signal voltage to the capacitor C1, and then the change-over switch 14 is turned off to be positioned at a neutral position as shown in FIG. 1 when the sample-and-hold pulse ϕ_{SH} becomes a low level or disappears at a time point t7 to thereby hold the signal voltage in the capacitor C1.

Thus, according to the above-described operation sequence, the signal charge of the n'th horizontal line is amplified by the amplifying MOSFET 4 and stored in the capacitor C1 of the CDS circuit 15, and thereafter, according to the similar operation sequence, the signal charge of the (n + 1)'th horizontal line is amplified by the amplifying MOSFET 4 corresponding to the (n + 1)'th line and stored in the capacitor C2 of the CDS circuit 15. Accordingly, the signal charges of the two pixels adjacent to each other in the vertical direction can be read out independently during an effective or valid horizontal scanning period by controlling the horizontal gateswitches 17_{-1} and 17_{-2}in response to the horizontal shift pulsesϕ_H applied from the horizontal scanning shift register 19. Now, in the effective horizontal scanning period, the reset gate (RG) is set at a high level and the reset drain (RD)

is set at a low level (about 1.5 V).

In the reading operation, a non-interlace television signal can be obtained by reading out the signal held in the capacitors C1 and C2 alternately. Alternatively, the signals held in the capacitors C1 and C2 may be read out simultaneously and then may be suitably processed by a signal processing system (not shown) to thereby obtain a non-interlace television signal similar to the sequential reading.

When the signal charge stored in the storage (ST) 1 overflows, it is dumped through a lateral overflow train passing from the storage ST to the reset drain RD through the output gate OG and the floating diffusion FD shown in FIG. 2. Accordingly, since the reset drain electrode (RD) of the MOSFET 3 for the reset operation is used not only for selecting the horizontal line but also for the overflow train, the circuit configuration for selecting the pixel of the horizontal line and that of the overflow train can be simplified.

As described above, according to the present invention, a noise cancelling unit is provided for the amplified outputs of the respective photo receptor portions of each vertical line so as to decrease noises such as the reset noise, the smear or the like, and further the solid state imager is configured to be the rear-illuminated structure, so that the sensitivity of the solid state imager can be improved due to the reduction of the noises and the numerical aperture thereof can be also improved.

Having described the preferred embodiment of the present invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to the precise embodiment and that various changes and modifications thereof could be effected by one skilled in the art without departing from the spirit or scope of the novel concepts of the invention as defined in the appended claims.

Claims

1. A solid state image comprising:
   (a) a plurality of pixels arranged in a matrix configuration and each having an amplifying element (4), the output of which is connected to a corresponding vertical signal line (9);
   (b) a plurality of noise cancel circuits (C_0)-,each being connected to a corresponding vertical signal line (9);
   (c) first hold means (C_1) for receiving the output signal of an n'th horizontal line during a horizontal blanking period through said noise cancel circuit (15);
   (d) second holding means (C_2) for receiving the output signal of a (n + 1)'th horizontal line during a horizontal blanking period through said noise cancel circuit (15); and
   (e) switching means (14) for selectively supplying the output signal of said noise cancel circuit (15) to said first hold means (C_1) or to said second hold means (C_2).

2. A solid state imager according to claim 1; wherein said amplifying element (4) is constituted by a metal oxide semiconductor field effect transistor.

3. A solid state imager according to claim 1, wherein said n'th horizontal line an (n + 1)'th horizontal line are selected by a vertical scanning shift register (8).

4. A solid state imager according to claim 3, wherein each of said plurality of pixels has a reset drain region for selecting said n'th horizontal line or said (n + 1)'th horizontal line in response to a reset drain pulse (ϕ_{RD}) applied thereto from said vertical scanning shift register (8).

5. A solid state imager according to claim 1, wherein each of said noise cancel circuits is constituted by a correlated double sampling circuit (15).

6. A solid state imager, comprising:
   (1) photo receptor portions (22) each provided for each of a plurality of pixels arranged in a matrix configuration in horizontal and vertical directions and each having an amplifying element (4) provided on a major surface side of a substrate (20) for amplifying a signal charge accumulated depending on the quantity of light incident thereon, said incident light being radiated on a rear surface side of said substrate;
   (2) noise cancelling means (15) each provided for each vertical line for cancelling a noise included in the output of the corresponding amplifying element (4);
   (3) first and second signal holding means (C_1, C_2) for holding during a horizontal blanking period amplified outputs of said photo receptor portions of two pixels adjacent to each other in the vertical direction passed through said noise cancelling means (15); and
   (4) signal reading means (14-17) for independently reading outputs of said first and second signal holding means.

7. A solid state imager according to claim 6, wherein the output signal of said signal reading

means is taken out from the rear side of said substrate.

8. A solid state imager according to claim 6, wherein a reset drain electrode (RD, 23) for dumping the signal charge stored in said photo receptor portion is formed on the rear surface side of said substrate.

FIG. 1

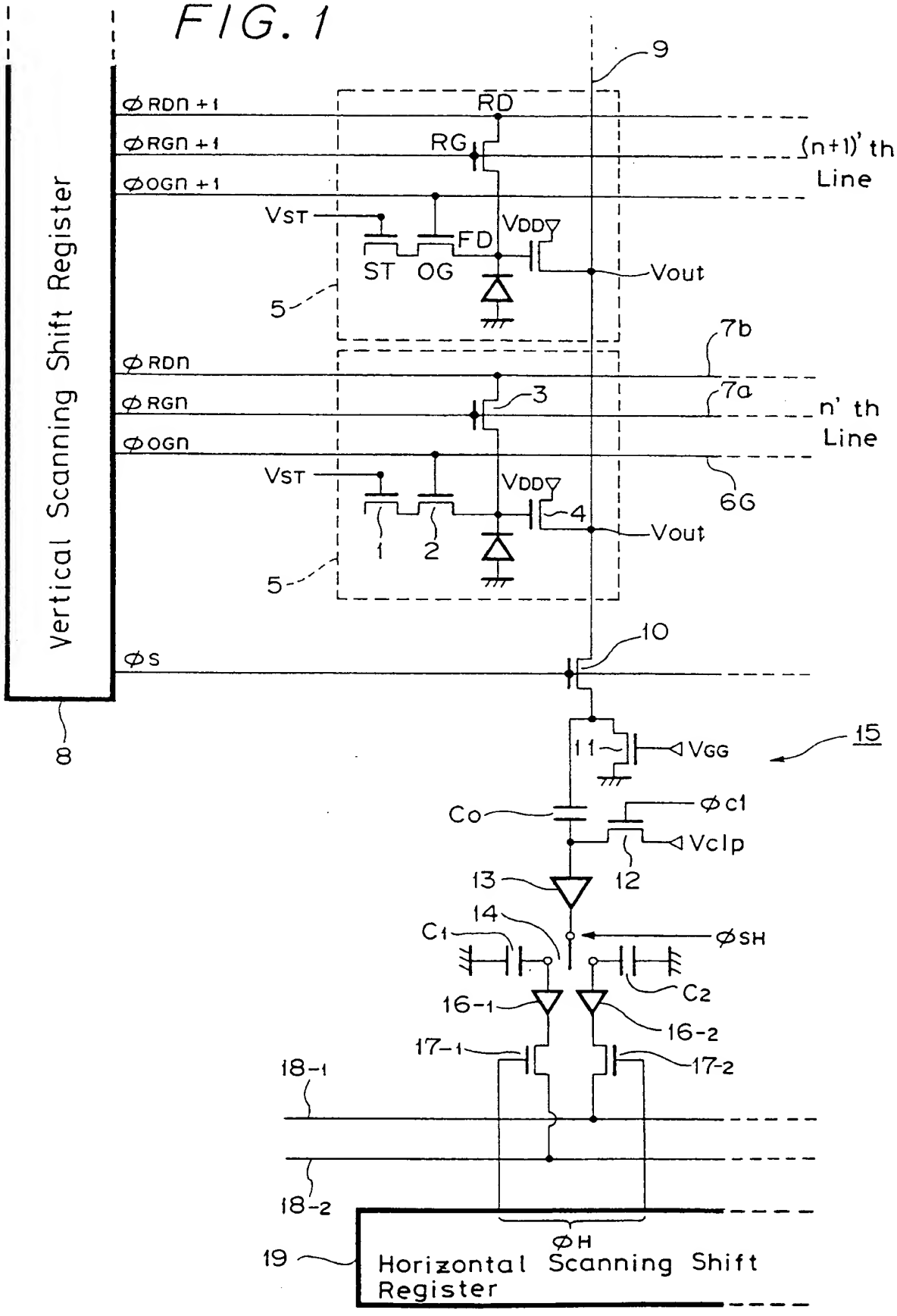

Vertical Scanning Shift Register
8
9
ØRDn+1
ØRGn+1
ØOGn+1
RD
RG
(n+1)' th Line
VST
FD
VDD
ST
OG
Vout
5
7b
ØRDn
ØRGn
ØOGn
3
7a
n' th Line
6G
VST
VDD
4
Vout
1
2
5
10
Øs
11
VGG
15
Co
Øc1
Vclp
12
13
14
C1
ØSH
C2
16-1
16-2
17-1
17-2
18-1
18-2
ØH
19
Horizontal Scanning Shift Register

FIG. 2

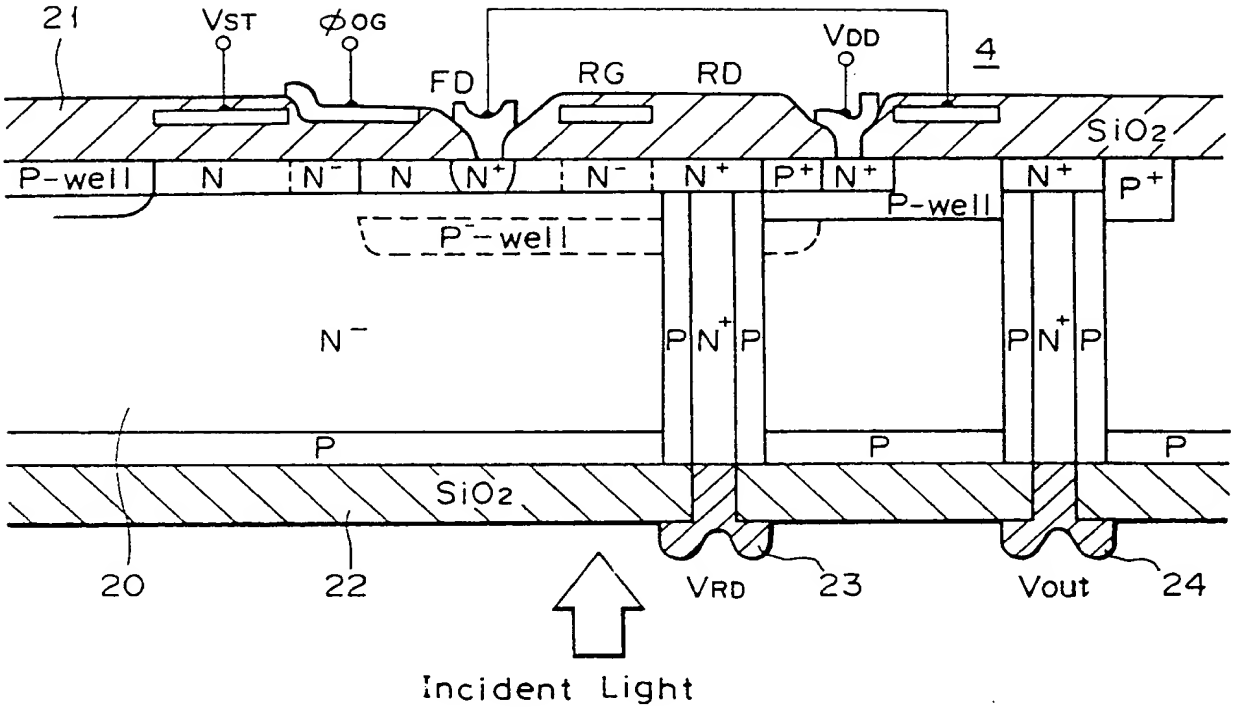
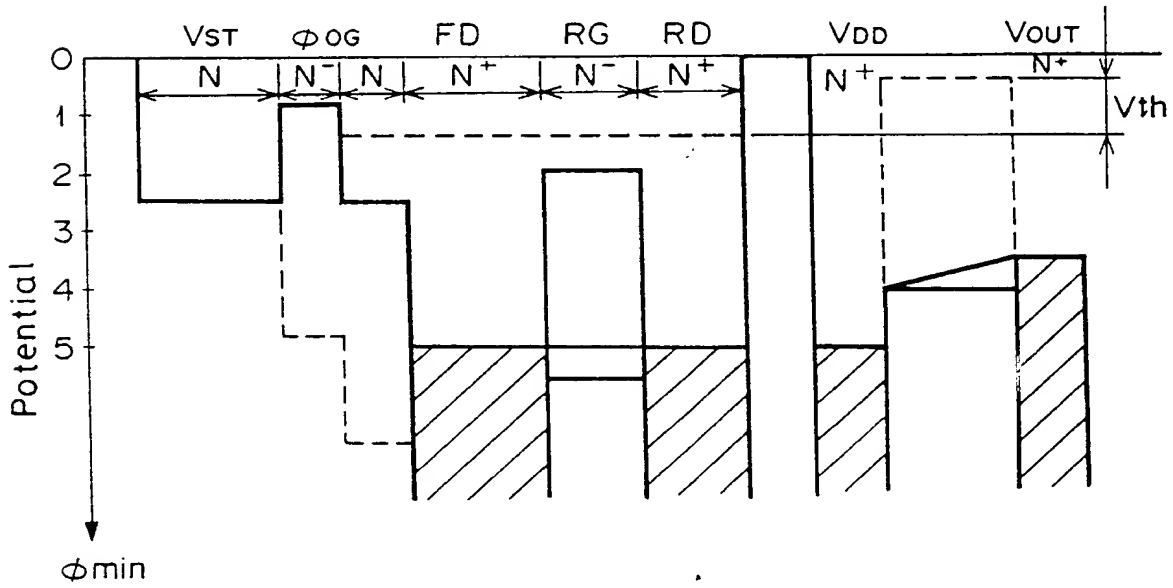

21
VST
φOG
FD
RG
RD
VDD
4
SiO2
P-well
N
N⁻
N
N⁺
N⁻
N⁺
P⁺
N⁺
P-well
N⁺
P⁺
P⁻-well
N⁻
P
N⁺
P
P
N⁺
P
P
P
P
SiO2
20
22
VRD
23
Vout
24
Incident Light

FIG. 3


VST
φOG
FD
RG
RD
VDD
VOUT
N
N⁻
N
N⁺
N⁻
N⁺
N⁺
N⁺
Vth
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1
2
3
4
5
Potential
φmin

FIG. 4

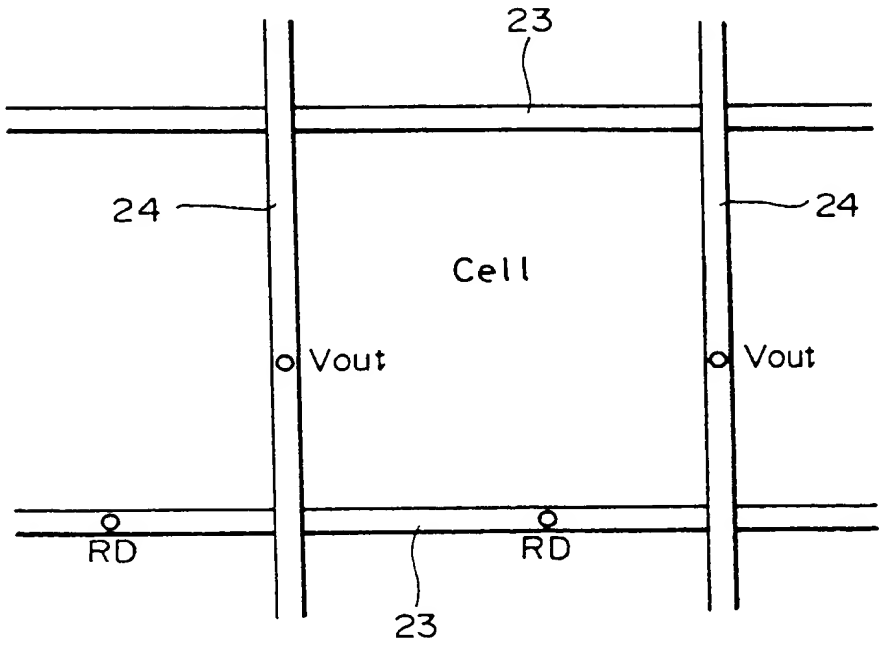

FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D

FIG. 5E

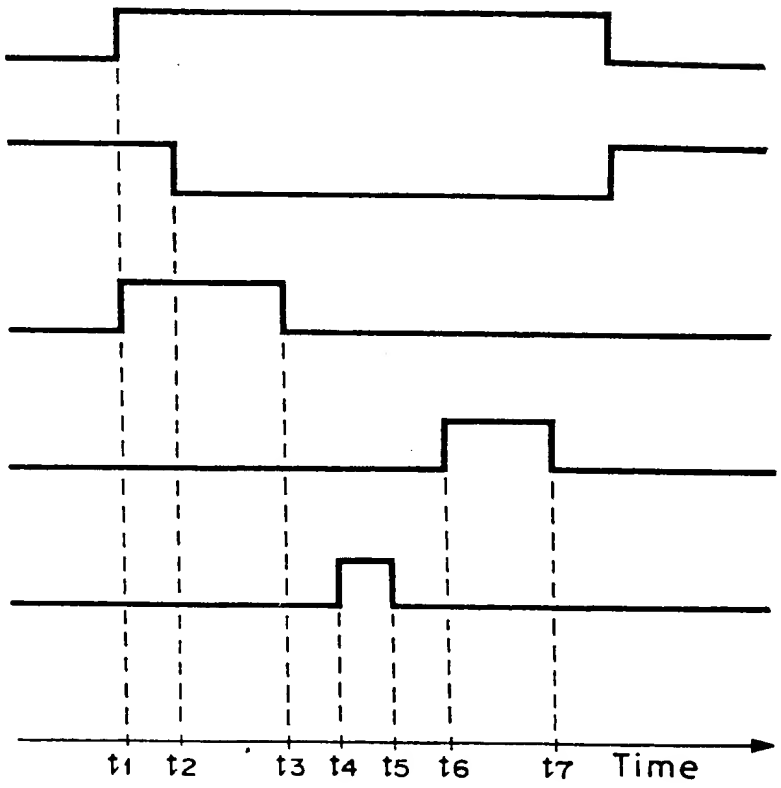

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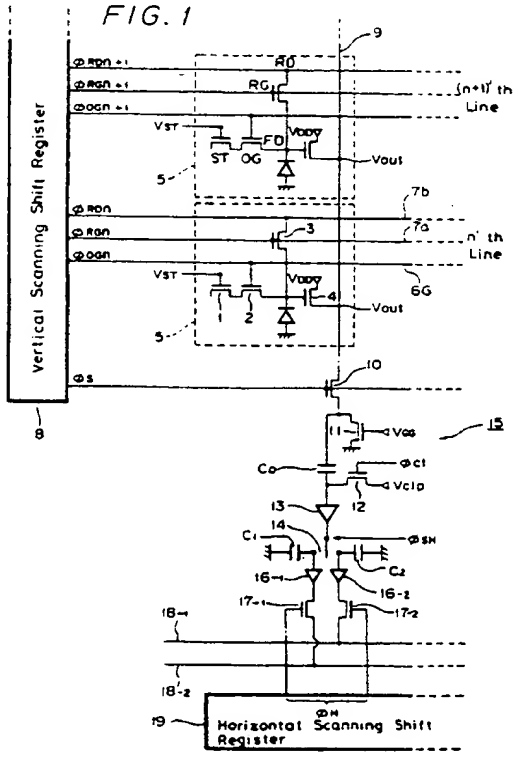
FIG. 1



EP 0 481 373 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 11 7396

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 942 474 (AKIMOTO et al.) * Figures 9,10; column 9, lines 41-64; column 11, lines 37-54 *	1-5	H 04 N 3/15
A		6	
P,A	EP-A-0 392 754 (CANON K.K.) * Figure 9; column 11, line 41 - column 12, line 32 *	1-5	
A	PATENT ABSTRACTS OF JAPAN, vol. 12, no. 308 (E-647), 22nd August 1988; & JP-A-63 076 367 (CANON INC.) 06-04-1988 * Whole document *	6	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 04 N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	05-03-1992	MONTANARI E.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

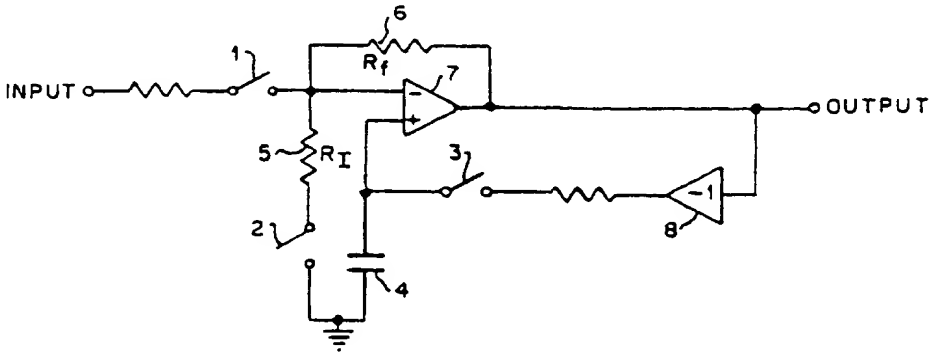
IBM Technical Disclosure Bulletin Vol. 23 No. 9 February 1981

XP-002052268

P.D.02-1981
p.4195-4196
2.
H03F 1/30D

DYNAMIC OFFSET NULL

W. J. Martin and M. J. Steinmetz



In certain types of precision operational amplifier circuits, the effects of the input offset error voltage of the operational amplifier must be minimized. The conventional approaches to the problem do not compensate for later drifts in the error voltage, or introduce additional sources of offset error which may become significant.

One method of nulling out the offset error dynamically is illustrated in the above circuit which depicts correction within a simple inverting amplifier. Normally, the circuit operates as an inverting amplifier with switches 2 and 3 open, and switch 1 closed. The voltage across capacitor 4 is so low as to be ignored in the calculations. During a nulling cycle, the positions of switches 1, 2, and 3 are reversed. In this mode, the ratio of resistors 5 and 6 are specified to produce a large gain by amplifier 7. The output of amplifier 7, in turn, comprises a voltage which is a large multiple of the input offset voltage applied to amplifier 8. Amplifier 8 is a unity gain inverter which inverts the output of amplifier 7 and applies it through switch 3 to the positive (+) input of amplifier 7. The steady-state voltage V_c produced at the positive input of amplifier 7 will be:

$$V_c = -\frac{(R_f + R_I)}{(R_f + 2R_I)} E_7 - \frac{R_I}{(R_f + 2R_I)} E_8$$

where E_7 and E_8 are the input offset errors of amplifiers 7 and 8, respectively. As the gain of amplifier 7 is set high ($R_f >> R_I$), the equation simplifies to:

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$$V_c = -E_7$$

thus completely cancelling the input offset error of amplifier 7. Capacitor 4 stores this voltage until the switches 1, 2, and 3 revert to their original states to permit amplifier 7 to perform its normal function.

By operating the circuit in this manner, all manual adjustments of the circuit are eliminated, and overall performance is improved without introducing additional offset errors into the circuit. This circuit has broad applicability in all types of operational amplifier configurations, and is not limited to the preferred embodiment herein described but has broader application in other operational amplifier circuits.

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